OIPE MAR 24 2008 PATENT & TRADEMARK OFFICE

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

March 19, 2008
Date

Beverly A. Loken
Beverly Loken

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Brent Keeth, Brian Johnson and Troy A. Manning	Attorney Docket No.:	500903.11
Patent No.	: US 6,882,579 B2	Serial No.	: 10/705,388
Issue Date	: April 19, 2005	Filed	: November 10, 2003
Title	: MEMORY DEVICE AND METHOD HAVING DATA PATH WITH MULTIPLE PREFETCH I/O CONFIGURATIONS		

REQUEST FOR CERTIFICATE OF CORRECTION

Certificate of Correction MAR 26 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Item (57), Line 2	"In either mode 32 bits"	--In either mode, 32 bits--
Column 1, Line 62	"or a low-speed,"	--or as low-speed,--
Column 3, Line 31	"which the"	--with the--
Column 3, Lines 44, 48, 49, 50, 52 and 53	"complimentary"	--complementary--
Column 3, Line 61	"terminals coupled serial	--terminals couple serial data-

RECEIVED CENTRAL FAX CENTER Patent MAR 26 2008

	data"	
Column 4, Line 3	"**54** FIG. 1) includes"	--**54** (FIG. **1**) includes--
Column 4, Lines 4, 6, 23, 30 and 33	"complimentary"	--complementary--
Column 4, Line 50	"flip-flips **120**"	--flip-flops **120**--
Column 5, Line 9	"coupled twice as many"	--couple twice as many--
Column 5, Lines 39, 42 and 60	"complimentary"	--complementary--
Column 5, Line 45	"It is for this reason, that this operating"	--It is for this reason that this operating--
Column 6, Line 16	"burst of 8 bits"	--bursts of 8 bits--
Column 6, Line 34	"**150***a* RinPar signal"	--**150***a* a RinPar signal--
Column 6, Line 52	"signal shift the"	--signal, shift the--
Column 6, Line 61	"compliment."	--complement.--
Column 8, Line 55	"data to or from 2N terminals of the memory device in form"	--data to or from 2N data bus terminals of the memory device in form--
Column 9, Line 9	"transferring a M*N data bits"	--transferring M*N data bits--
Column 10, Line 19	"transferring a M*N data bits"	--transferring M*N data bits--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

RECEIVED-USPTO
Publication
MAR 26 2008

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: March 18, 2008

By: Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847
Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
(206) 903-8785
Attorney for Applicant(s)

EWB:tdp

Enclosures:
Postcard
Form PTO-1050 (+ copy)

500903.11 req cert correct

RECEIVED-USPTO
Patent Publication
MAR 26 2008

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

March 19, 2008 — Date

Beverly A. Loken — Beverly Loken

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Brent Keeth, Brian Johnson and Troy A. Manning	Attorney Docket No.:	500903.11
Patent No.	: US 6,882,579 B2	Serial No.	: 10/705,388
Issue Date	: April 19, 2005	Filed	: November 10, 2003
Title	: MEMORY DEVICE AND METHOD HAVING DATA PATH WITH MULTIPLE PREFETCH I/O CONFIGURATIONS		

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Item (57), Line 2	"In either mode 32 bits"	--In either mode, 32 bits--
Column 1, Line 62	"or a low-speed,"	--or as low-speed,--
Column 3, Line 31	"which the"	--with the--
Column 3, Lines 44, 48, 49, 50, 52 and 53	"complimentary"	--complementary--
Column 3, Line 61	"terminals coupled serial	--terminals couple serial data--

MAR 26 2008

	data"	
Column 4, Line 3	"**54** FIG. **1**) includes"	--**54** (FIG. **1**) includes--
Column 4, Lines 4, 6, 23, 30 and 33	"complimentary"	--complementary--
Column 4, Line 50	"flip-flips **120**"	--flip-flops **120**--
Column 5, Line 9	"coupled twice as many"	--couple twice as many--
Column 5, Lines 39, 42 and 60	"complimentary"	--complementary--
Column 5, Line 45	"It is for this reason, that this operating"	--It is for this reason that this operating--
Column 6, Line 16	"burst of 8 bits"	--bursts of 8 bits--
Column 6, Line 34	"**150***a* RinPar signal"	--**150***a* a RinPar signal--
Column 6, Line 52	"signal shift the"	--signal, shift the--
Column 6, Line 61	"compliment."	--complement.--
Column 8, Line 55	"data to or from 2N terminals of the memory device in form"	--data to or from 2N data bus terminals of the memory device in form--
Column 9, Line 9	"transferring a M*N data bits"	--transferring M*N data bits--
Column 10, Line 19	"transferring a M*N data bits"	--transferring M*N data bits--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

RECEIVED-USPTO
Patent Publication

MAR 2 6 2008

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: March 18, 2008

By: Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847
Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
(206) 903-8785
Attorney for Applicant(s)

EWB:tdp

Enclosures:
Postcard
Form PTO-1050 (+ copy)

500903.11 req cert correct

RECEIVED USPTO
Patent Publication
MAR 26 2008

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : US 6,882,579 B2
DATED : April 19, 2005
INVENTOR(S) : Brent Keeth, Brian Johnson and Troy A. Manning

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Item (57), Line 2	"In either mode 32 bits"	--In either mode, 32 bits--
Column 1, Line 62	"or a low-speed,"	--or as low-speed,--
Column 3, Line 31	"which the"	--with the--
Column 3, Lines 44, 48, 49, 50, 52 and 53	"complimentary"	--complementary--
Column 3, Line 61	"terminals coupled serial data"	--terminals couple serial data--
Column 4, Line 3	"**54** FIG. 1) includes"	--**54** (FIG. 1) includes--
Column 4, Lines 4, 6, 23, 30 and 33	"complimentary"	--complementary--
Column 4, Line 50	"flip-flips **120**"	--flip-flops **120**--
Column 5, Line 9	"coupled twice as many"	--couple twice as many--
Column 5, Lines 39, 42 and 60	"complimentary"	--complementary--
Column 5, Line 45	"It is for this reason, that this operating"	--It is for this reason that this operating--
Column 6, Line 16	"burst of 8 bits"	--bursts of 8 bits--
Column 6, Line 34	"**150***a* RinPar signal"	--**150***a* a RinPar signal--
Column 6, Line 52	"signal shift the"	--signal, shift the--
Column 6, Line 61	"compliment."	--complement.--
Column 8, Line 55	"data to or from 2N terminals of the memory device in form"	--data to or from 2N data bus terminals of the memory device in form--
Column 9, Line 9	"transferring a M*N data bits"	--transferring M*N data bits--

MAR 2 6 2008

Column 10, Line 19	"transferring a M*N data bits"	--transferring M*N data bits--

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101

Patent No. US 6,882,579 B2

No. add'l. copies
@ .30 per page
➔ _____

FORM PTO-1050 (REV. 3-82)
500903.11 PTO 1050

RECEIVED-USPTO
Patent Publication
MAR 26 2008

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : US 6,882,579 B2
DATED : April 19, 2005
INVENTOR(S) : Brent Keeth, Brian Johnson and Troy A. Manning

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Item (57), Line 2	"In either mode 32 bits"	--In either mode, 32 bits--
Column 1, Line 62	"or a low-speed,"	--or as low-speed,--
Column 3, Line 31	"which the"	--with the--
Column 3, Lines 44, 48, 49, 50, 52 and 53	"complimentary"	--complementary--
Column 3, Line 61	"terminals coupled serial data"	--terminals couple serial data--
Column 4, Line 3	"**54** FIG. **1**) includes"	--**54** (FIG. **1**) includes--
Column 4, Lines 4, 6, 23, 30 and 33	"complimentary"	--complementary--
Column 4, Line 50	"flip-flips **120**"	--flip-flops **120**--
Column 5, Line 9	"coupled twice as many"	--couple twice as many--
Column 5, Lines 39, 42 and 60	"complimentary"	--complementary--
Column 5, Line 45	"It is for this reason, that this operating"	--It is for this reason that this operating--
Column 6, Line 16	"burst of 8 bits"	--bursts of 8 bits--
Column 6, Line 34	"**150***a* RinPar signal"	--**150***a* a RinPar signal--
Column 6, Line 52	"signal shift the"	--signal, shift the--
Column 6, Line 61	"compliment."	--complement.--
Column 8, Line 55	"data to or from 2N terminals of the memory device in form"	--data to or from 2N data bus terminals of the memory device in form--
Column 9, Line 9	"transferring a M*N data bits"	--transferring M*N data bits--

RECEIVED-USPTO
MAR 2 6 2008
RECEIVED-USPTO
MAR 2 6 2008

Column 10, Line 19	"transferring a M*N data bits"	--transferring M*N data bits--

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101

Patent No. US 6,882,579 B2

No. add'l. copies
@ .30 per page
➔ _____

FORM PTO-1050 (REV. 3-82)
500903.11 PTO 1050

RECEIVED-USPTO
MAR 2 6 2008